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PATENT & TRADEMARK OFFICE

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DOCKET NO.: 4284

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN THE MATTER OF THE PATENT

OF: Matthias EICHIN et al.

PATENT NO.: 6,937,048

ISSUE DATE: August 30, 2005

FOR: METHOD FOR TESTING AN INTEGRATED CIRCUIT WITH AN EXTERNAL POTENTIAL APPLIED TO A SIGNAL OUTPUT PIN

COMMISSIONER FOR PATENTS
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450

November 9, 2005

REQUEST FOR THE ISSUANCE OF A CERTIFICATE OF CORRECTION UNDER 35 USC 254 AND CERTIFICATE OF MAILING

Dear Sir:

1) The above identified Patent contains printing errors by the USPTO. Please correct the errors as shown on the enclosed Form PTO-1050. For an explanation of the requested changes, please see our Response dated June 17, 2003 at page 4 lines 1 and 3, page 5 line 7, page 7 line 12, and page 16; the Replacement Sheets of drawings filed on September 22, 2003; as well as the Examiner's Amendment of April 20, 2005, 1.c).

2) Issuance of a Certificate of Correction as soon as possible will be much appreciated.

Respectfully submitted,
Matthias EICHIN et al. - Patentee

By _____
Walter F. Fasse
Patent Attorney
Reg. No.: 36132
Tel. No.: 207-862-4671
Fax. No.: 207-862-4681
P.O. Box 726
Hampden, Maine 04444-0726

WFF:ks/4284
Enclosures:
postcard,
Form PTO-1050 (2x),
copy of Replacement Sheet

CERTIFICATE OF MAILING:
I hereby certify that this correspondence with all indicated enclosures is being deposited with the U. S. Postal Service with sufficient postage as first-class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

Karin Smith - November 9, 2005
Name: Karin Smith - Date: November 9, 2005

Certificate
NOV 17 2005
of Correction
NOV 17 2005

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,937,048

DATED : August 30, 2005

INVENTOR(S) : Eichin et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page,
Item [57], ABSTRACT,
Delete and replace the Abstract to read as follows:

--An integrated circuit can be tested externally without requiring additional testing output pins or test measuring pads. In the new method, the circuit functions are tested by using the output pins at which the output signal is present during normal operation of the integrated circuit. A defined voltage value is applied to the signal output pin. An integrated control unit evaluates the applied voltage value, and in response thereto switches the integrated circuit into a test mode in which it applies selected signals, which are to be tested, at the signal output pin.--;

In the Drawings
Replace sheet 3 with the attached Replacement Sheet bearing formal Fig. 3;

Column 3,
Line 34, after "value", replace "Bet" by --set--;
Line 37, after "window", delete --of the--;

Column 4,
Line 24, after "line", delete --,--;
Line 53, after "unchanged", replace "acceptionally" by --or optionally--;

Column 5,
Line 49, after "SE1", insert --(MS)--.

ADDRESS OF SENDER: FASSE PATENT ATTORNEYS, P.A.
P. O. BOX 726
Hampden, Maine 04444-0726 U.S.A.

Form PTO 1050 (REV.3-82)

NOV 17 2005

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Form PTO 1050 (REV.3-82)

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US Pat 6,937,048

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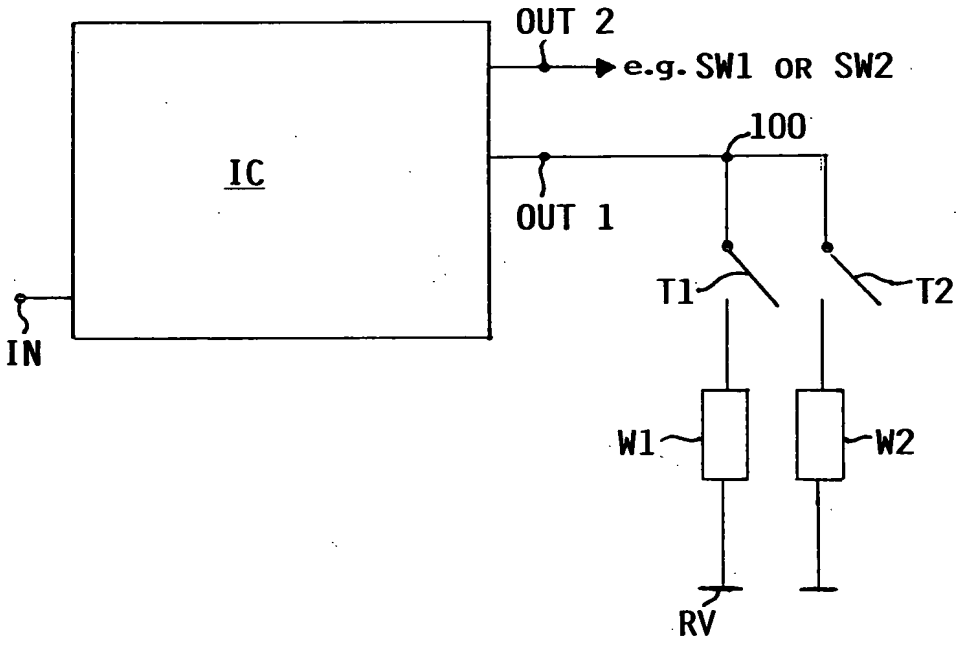

FIG. 3

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